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(54) High-frequency semiconductor device

(57) A drain electrode (31) and a source electrode (29) are provided for an intrinsic device section (22) on a GaAs substrate (21) with a gate electrode (36) placed therebetween. Almost the entire area of the GaAs substrate (21) is covered by an extending source electrode (30) extending from the source electrode (29). A belt-shaped extending drain electrode (39) is provided on the source electrode (29) with a dielectric layer (34) placed therebetween, and thereby an output-side microstripline (40B) is formed. A belt-shaped extending gate electrode (35) is also provided on the source electrode (29) with a dielectric layer (34) placed therebetween, and thereby an input-side microstripline (40A) is formed.

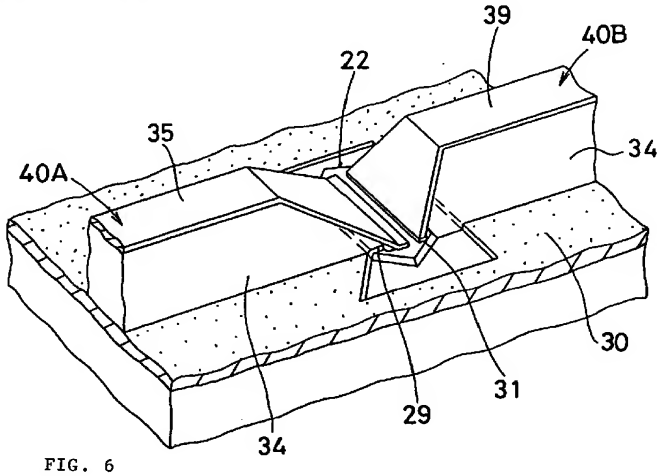

FIG. 6

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to high-frequency semiconductor devices. The present invention more particularly relates to a high-frequency field effect transistor (FET) used for a millimetric-wave or quasi-millimetric-wave circuit module for amplification, oscillation, and modulation.

2. Description of the Related Art

Fig. 1 is a plan showing a structure of an electrode formed on a semiconductor surface in a currently well used high-frequency FET serving as a conventional FET. In this high-frequency FET, three source electrodes 2 extend from a source pad section 1 and two drain electrodes 4 extending from a drain pad section 3 are disposed between the source electrodes 2. Four very narrow gate electrodes 6 extending from two gate pad sections 5 disposed between the tips of the drain electrodes 4 and the source pad section 1 extend long and narrowly in areas sandwiched by the source electrodes 2 and the drain electrodes 4. In other words, this high-frequency FET is a horizontal-type (plane-type) FET in which the source electrodes 2, the gate electrodes 6, and the drain electrodes 4 are formed on the same plane.

To make such an FET usable in higher frequencies, it is necessary to reduce the distance between the source electrode and the drain electrode and to narrow the gate electrode (reduce the gate length). A narrow and long gate electrode has large parasitic resistance and parasitic capacitance, however, and thereby the characteristics deteriorate by noise increase, operating-frequency decrease, gain reduction, and increased input/output reflection loss.

When the FET is viewed as a waveguide in which a micro wave transmits, it has a very unusual structure and its operating range is limited to a low frequency zone in which the FET can be approximated to a lumped-constant circuit device.

Fig. 2 is a plan illustrating an electrode structure of an air-bridge-gate-structure FET which improves the above characteristics deterioration. In this structure, a source electrode 8 disposed between source pad sections 7 on a semiconductor surface faces a drain electrode 9 at its full length, a wide gate electrode 11 extends over the source electrode 8 from a gate pad section 10 disposed at the side opposite the drain electrode 9 against the source electrode 8, and the tip edge of the gate electrode 11 is Schottky-connected to the semiconductor surface between the source electrode 8 and the drain electrode 9.

Since the gate electrode 11 can be made wide in such an air-bridge-gate-structure FET, the parasitic resistance and the parasitic inductance of the gate electrode 11 are reduced and the RF characteristics (especially noise characteristics) are improved.

At a portion where the gate electrode 11 passes over the source electrode 8, a parasitic capacitor is generated between the source electrode 8 and the gate electrode 11, and the operating frequency decreases. To reduce this parasitic capacitance, the source electrode 8 needs to be narrowed. If the source electrode 8 is narrowed, since the source electrode 8 has additional parasitic resistance and additional parasitic inductance, characteristics improvement is limited in such a method.

When this air-bridge-gate-structure FET is viewed as a waveguide, it has a very unusual structure like a horizontal-type FET, and its operating range is limited to a low frequency zone in which the FET can be approximated to a lumped-constant circuit device.

To solve a characteristics deterioration problem of a high-frequency FET in millimetric-wave and quasi-millimetric-wave ranges, it is an important issue to eliminate wiring resistors and parasitic components such as parasitic capacitors and parasitic inductors in the gate electrode and the drain electrode, as described above. It is very difficult, however, to suppress characteristics deterioration in a high-frequency range in a conventional FET structure, and a semiconductor device suited to a millimetric wave and a quasi-millimetric wave cannot be manufactured.

SUMMARY OF THE INVENTION

The present invention is made in consideration of the above-described drawbacks in a conventional device. Accordingly, it is an object of the present invention to suppress characteristics deterioration of a semiconductor device in a high-frequency range by using the structure of a micro-wave transmission line for electrode structures between the gate electrode and the source electrode and between the drain electrode and the source electrode.

The foregoing object is achieved according to one aspect of the invention through the provision of a high-frequency semiconductor device, wherein an intrinsic device section is partially formed on a semiconductor substrate; a source electrode and a drain electrode are disposed in the intrinsic device section with a gate electrode placed therebetween; a micro-wave transmission line is formed between the gate electrode or an electrode section electrically connected to the gate electrode and the source electrode or an electrode section electrically connected to the source electrode; and a micro-wave transmission line is formed between the drain electrode or an electrode section electrically connected to the drain electrode and the source electrode or an electrode section electrically connected to the source electrode.

In a high-frequency semiconductor device accord-

ing to the present invention, since a micro-wave transmission line is formed between the drain electrode or an electrode section electrically connected to the drain electrode and the source electrode or an electrode section electrically connected to the source electrode and a micro-wave transmission line is formed between the gate electrode or an electrode section electrically connected to the gate electrode and the source electrode or an electrode section electrically connected to the source electrode, parasitic components between the gate and source electrodes and between the drain and source electrodes can be reduced and the characteristics of the high-frequency semiconductor device can be improved.

The foregoing object is also achieved according to another aspect of the invention through the provision of a high-frequency semiconductor device, wherein an intrinsic device section is partially formed on a semiconductor substrate; a source electrode and a drain electrode are disposed in the intrinsic device section with a gate electrode placed therebetween; the source electrode or an electrode section electrically connected to the source electrode covers most of the semiconductor substrate; a micro-wave transmission line is formed by oppositely disposing the gate electrode or an electrode section electrically connected to the gate electrode through a dielectric layer above the source electrode or an electrode section electrically connected to the source electrode; and a micro-wave transmission line is formed by oppositely disposing the drain electrode or an electrode section electrically connected to the drain electrode through a dielectric layer above the source electrode or an electrode section electrically connected to the source electrode.

Any types of micro-wave transmission lines can be used, such as a microstripline, a slot line, and a coplanar line. In the high-frequency semiconductor device described above, the source electrode opposes the drain electrode with the dielectric layer disposed therebetween, or the source electrode opposes the gate electrode with the dielectric layer disposed therebetween to form a micro-wave transmission line similar to a microstripline.

The high-frequency semiconductor devices described above may be configured such that a plurality of the intrinsic device sections are disposed on the semiconductor substrate and the plurality of the intrinsic device sections are connected by micro-wave transmission lines.

In such a high-frequency semiconductor device, since a plurality of intrinsic device sections are disposed and they are connected with micro-wave transmission lines, a larger output power is obtained than in a single intrinsic device section.

In a high-frequency semiconductor device according to the present invention, since a micro-wave transmission line serves as a connection portion of an intrinsic device section, an input signal transfers through a waveguide without disturbing an electromagnetic field distribution. Therefore, drawbacks caused by parasitic inductance or parasitic capacitance in a semiconductor device having a conventional structure can be eliminated. According to the present invention, a low-noise millimetric-wave semiconductor device having a high power gain and high operating frequencies is obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan showing an electrode structure in a conventional horizontal-type FET.

Fig. 2 is a plan showing an electrode structure in a conventional FET having an air bridge gate structure.

Fig. 3 is a plan showing a structure of a high-frequency semiconductor device according to one embodiment of the present invention.

Fig. 4 is a cross section taken on line X1-X1 shown in Fig. 3.

Fig. 5 is a cross section taken on line X2-X2 shown in Fig. 4.

Fig. 6 is a perspective view showing a structure of the vicinity of an intrinsic device section in the semiconductor device.

Fig. 7 is a partially broken plan showing a state in which the semiconductor device is mounted on a circuit board.

Fig. 8A is a plan showing a structure of a high-frequency semiconductor device according to another embodiment of the present invention. Fig. 8B is a cross section taken on line X3-X3 shown in Fig. 8A.

Fig. 9 is a plan of a high-frequency semiconductor device according to still another embodiment of the present invention.

Fig. 10 is a plan showing a structure of a high-frequency semiconductor device according to yet another embodiment of the present invention.

Fig. 11 is a chart showing the gain difference between a device having a single-stage intrinsic device section (FET structure) and a device having two-stage intrinsic device sections.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First embodiment

Fig. 3 is a plan showing a structure of a high-frequency semiconductor device (high-frequency FET) 21 according to one embodiment of the present invention. Fig. 4 is a cross section taken on line X1-X1 shown in Fig. 3, and Fig. 5 is a cross section taken on X2-X2 shown in Fig. 3. Fig. 6 is a perspective view showing a structure of the vicinity of an intrinsic device section 22 of the high-frequency semiconductor device 21.

On a semi-insulating GaAs substrate (GaAs wafer) 23, a buffer layer 24 made from undoped-GaAs, a channel layer (active layer) 25 made from n-InGaAs, and an

insulating layer 26 made from undoped-AlGaAs are epitaxially grown by the molecular beam epitaxitial (MBE) method, and etched in a hexagonal shape to form a mesa-type intrinsic device section 22. The buffer layer 24 covers the surface of the GaAs substrate 23. At both ends of the insulating layer 26, n-type impurities are injected such that they reach the channel layer 25, to form an n-type source area 27 and an n-type drain area 28.

At a slope of the intrinsic device section 22 made from the buffer layer 24, the channel layer 25, and the insulating layer 26, a source electrode 29 ohmic-contacts the source area 27 with an electrode material such as Au/Ge. An extending source electrode 30 is formed at almost the entire area on the buffer layer 24 except the intrinsic device section 22. The extending source electrode 30 is electrically connected to the source electrode 29 and contacts the source area 27 through the source electrode 29.

A drain electrode 31 ohmic-contacts the drain area 28 in the intrinsic device section 22. The extending source electrode 30 is not placed partially at the output side and the buffer layer 24 is exposed there. A drain pad section 37 is formed at that position. Under the drain pad section 37, an electrically conductive via hole 38 is formed. From the intrinsic device section 22 to the drain pad section 37, a belt-shaped dielectric layer 34 about 10 μm thick and about 25 μm wide is formed by SiO_2, SiN, and PSG. An extending drain electrode 39 is formed in a belt shape on the upper surface of the dielectric layer 34, and is connected to the drain electrode 31 and the drain pad section 37 at both ends.

On the upper surface of the intrinsic device section 22, a mushroom-shaped gate electrode 36 is formed by an electrode material such as TiN such that it is Schottky-connected to the insulating layer 26. The extending source electrode 30 is not placed partially at the input side and the buffer layer 24 is exposed there. A gate pad section 32 is formed at that position. Under the gate pad section 32, an electrically conductive via hole 33 is formed. From the intrinsic device section 22 to the gate pad section 32, a belt-shaped dielectric layer 34 about 10 μm thick and about 25 μm wide is formed by SiO_2, SiN, and PSG. An extending gate electrode 35 is formed in a belt shape on the upper surface of the dielectric layer 34, and is connected to the gate electrode 36 and the gate pad section 32 at both ends.

An input-side microstripline 40A is formed by the extending source electrode 30 and the extending gate electrode 35 formed thereabove with the dielectric layer 34 placed therebetween. In the same way, an output-side microstripline 40B is formed by the extending source electrode 30 and the extending drain electrode 39 formed thereabove with the dielectric layer 34 placed therebetween.

At ends of the input and output sides, via holes 41 and 42 electrically connected to the extending source electrode 30 are formed.

(Operations in the present embodiment)

In the high-frequency semiconductor device 21 manufactured in this way, the intrinsic device section 22 has an FET structure in which the source electrode 29 and the drain electrode 31 are disposed with the gate electrode 36 placed therebetween.

The high-frequency semiconductor device 21 can be connected to a circuit board 43 having coplanar lines 47A and 47B as shown in Fig. 7. The input-side microstripline 40A of the semiconductor device 21 is connected to the input-side coplanar line 47A of the circuit board 43 by connecting the via holes 41, which are electrically connected to the input-side extending source electrode 30, to a ground conductor 44 of the input-side coplanar line 47A in the circuit board 43, and by connecting the via hole 33, which is electrically connected to the extending gate electrode 35, to the strip conductor 45 of the coplanar line 47A. In the same way, the output-side microstripline 40B of the semiconductor device 21 is connected to the output-side coplanar line 47B of the circuit board 43 by connecting the via holes 42, which are electrically connected to the output-side extending source electrode 30, to the ground conductor 44 of the output-side coplanar line 47B in the circuit board 43 and by connecting the via hole 38, which is electrically connected to the extending drain electrode 39, to the strip conductor 46 of the coplanar line 47B. Therefore, at the input side of the semiconductor device 21, among electrodes constituting the microstripline 40A and sandwiching the dielectric layer 34, the extending source electrode 30 serves as an RF-ground electrode and the extending gate electrode 35 serves as an RF signal line. In the same way at the output side, among electrodes constituting the microstripline 40B and sandwiching the dielectric layer 34, the extending source electrode 30 serves as an RF-ground electrode and the extending drain electrode 39 serves as an RF signal line.

As described above, by inputting/outputting a signal from the lower surface of the GaAs substrate 23 through the via holes 33, 41, 38, and 42, noise and signal leakage caused by parasitic coupling between the coplanar lines 47A and 47B of the circuit board 43 and the microstriplines 40A and 40B of the high-frequency semiconductor device 21 are reduced.

The characteristic impedance of each of the microstriplines 40A and 40B at both input and output matches that of the intrinsic device section 22. In other words, the line width and the line height (namely, the widths of the extending gate electrode 35 and the extending drain electrode 39 and the thickness of the dielectric layer 34) of the microstriplines 40A and 40B for input and output are designed such that the characteristic impedance is substantially equal to the input and output impedance of the intrinsic device section 22 in the millimetric wave band and the matching conditions are satisfied. When the microstriplines 40A and 40B 10 μm thick and 25 μm

wide are formed by use of a dielectric layer 34 having a relative dielectric constant ε of 2.5 to 5.0, for example, a characteristic impedance of 40 to 70 Ω is obtained. This characteristic impedance is substantially equal to the input and output impedance of an intrinsic device section 22 having a gate width of 30 to 60 μm in the millimetric wave band, and the matching conditions are satisfied.

An RF signal (electromagnetic wave) input to the input-side microstripline 40A through the via holes 33 and 41 from the coplanar line 47A of the circuit board 43 is transferred through the microstripline 40A to reach the intrinsic device section 22. The RF signal to which signal processing such as amplification is applied in the intrinsic device section 22 is transferred through the microstripline 40B, and sent to the coplanar line 47B of the circuit board 43 through the via holes 38 and 42.

(Features of the present embodiment)

A method for improving the performance of the high-frequency semiconductor device 21 is to reduce coupling in electromagnetic fields between the extending gate electrode 35 and the extending source electrode 30 and between the extending gate electrode 35 and the extending drain electrode 39. In a conventional horizontal-type FET, electrodes are formed such that they do not intersect (see Fig. 1), or electrodes are formed such that the intersections of electrodes become as small as possible (see Fig. 2). In contrast, in the high-frequency semiconductor device 21 according to the present invention, by active use of coupling between the extending gate electrode 35 and the extending source electrode 30, and between the extending drain electrode 39 and the extending source electrode 30, these input and output electrodes are made using microstrip-conductor-type waveguide structures to reduce parasitic coupling components (parasitic inductance and parasitic capacitance) of the extending gate electrode 35 and the extending drain electrode 39. In other words, since an RF signal transfers in phase through the input and output microstriplines 40A and 40B between the upper and lower electrodes, parasitic coupling between the upper and lower electrodes does not substantially exist.

Second embodiment

Fig. 8A is a plan of a high-frequency semiconductor device 51 according to another embodiment of the present invention. Fig. 8B is a cross section taken on line X3-X3 shown in Fig. 8A. In this high-frequency semiconductor device 51, a ground conductor 52 is provided in parallel to an input-side edge of an extending source electrode 30 to form an input-side slot line 54A between the edge of the extending source electrode 30 and the ground conductor 52. The input-side slot line 54A is connected to an input-side microstripline 40A at a right angle so that the slot line 54A and the microstripline 40A are electromagnetically coupled. In the same way, a ground conductor 53 is provided in parallel to an output-side edge of the extending source electrode 30 to form an output-side slot line 54B between the edge of the extending source electrode 30 and the ground conductor 53. The output-side slot line 54B is connected to an output-side microstripline 40B at a right angle so that the slot line 54B and the microstripline 40B are electromagnetically coupled. Via holes 55 and 56 are electrically connected to the ground conductors 52 and 53, respectively.

An RF signal input to the slot line 54A transmits to an intrinsic device section 22 through the microstripline 40A. An RF signal output from the intrinsic device section 22 passes through the microstripline 40B and is output from the slot line 54B.

Since the slot lines 54A and 54B can be connected to slot lines on a circuit board through via holes 41 and 54, and 42 and 56, respectively, the device is easily connected to the circuit board formed by slot lines.

Third embodiment

Fig. 9 is a plan of a high-frequency semiconductor device 61 according to still another embodiment of the present invention. In this embodiment, two intrinsic device sections 22 are formed with an appropriate distance being left therebetween, and microstriplines 40A and 40B are formed at the input and output sides of each intrinsic device section 22, respectively. A Y-shaped branched input-side slot line 62 is formed between an extending source electrode 30 and a ground electrode 64, and each branched section of the slot line 62 is electromagnetically coupled with an input-side microstripline 40A. When they are coupled at the point away from a tip of the slot line 62 by $\lambda/4$ (where λ indicates the wavelength of an electromagnetic wave), the maximum coupling is obtained. In the same way, a Y-shaped branched output-side slot line 63 is formed between the extending source electrode 30 and the ground electrode 64, and each branched section of the slot line 63 is electromagnetically coupled with an output-side microstripline 40B. A via hole 65 is electrically connected to the center section of the extending source electrode, via holes 66 are electrically connected to the ground conductor 64 at the input side, and via holes 67 are electrically connected to the ground conductor 64 at the output side.

In this embodiment, an RF signal input to the slot line 62 at the input end is divided in the slot line 62, transfers to a microstripline 40A, and is input to each intrinsic device section 22. An RF signal output from the intrinsic device section 22 transfers through a microstripline 40B to the slot line 63, is combined in the slot line 63, and output from the slot line 63. Therefore, even in this embodiment, larger output power can be obtained than that of a semiconductor device having a

single intrinsic device section.

Since a gate electrode 36 and a drain electrode 31 are connected to each intrinsic device section 22 with wide wiring patterns, the resistance of each electrode is suppressed to a low level.

Fourth embodiment

Fig. 10 is a plan of a high-frequency semiconductor device 71 according to yet another embodiment of the present invention. In this embodiment, a plurality of intrinsic device sections 22a and 22b are connected in series. Since different voltages are applied to the drain electrode 31 of a first-stage intrinsic device section 22a and to the gate electrode 36 of a second-stage intrinsic device section 22b, an extending drain electrode 39 of the first-stage intrinsic device section 22a and an extending gate electrode 35 of the second-stage intrinsic device section 22b are capacitive coupled through a dielectric layer 34 by a direct-current-cut thin-film opposing capacitor structure 72. Therefore, the first-stage intrinsic device section 22a and the second-stage intrinsic device section 22b are connected with a microstripline 40C having the thin-film capacitor structure 72.

The same thin-film capacitor structure 72 is formed at an extending gate electrode 35 of the first-stage intrinsic device section 22a. A gate pad section 32 and the first intrinsic device section 22a are connected with a microstripline 40A having the thin-film capacitor structure 72. The same thin-film capacitor structure 72 is also formed at an extending drain electrode 39 of the second-stage intrinsic device section 22b. The second-stage intrinsic device section 22b and the drain pad section 37 are connected with a microstripline 40B having the thin-film capacitor structure 72.

At the input and output sections of the semiconductor device 71, slot lines 73A and 73B are formed by portions where the extending source electrode 30 is not formed. The input-side slot line 73A is electromagnetically coupled with the input-side microstripline 40A, and the output-side slot line 73B is electromagnetically coupled with the output-side microstripline 40B.

A gate bias line 74 used for applying a DC bias to the gate electrode 36 extends from a pad 76 provided on a via hole 75 at a portion where the extending source electrode 30 is not formed, to the gate electrode 36. In the same way, a drain bias line 77 used for applying a DC bias to the drain electrode 31 extends from a pad 79 provided on a via hole 78 at a portion where the extending source electrode 30 is not formed, to the drain electrode 31. The gate bias line 74 and the drain bias line 77 pass under a buffer layer 24 below the lower surface of the extending source electrode 30, and are insulated from the extending source electrode 30. They may be insulated from the extending source electrode 30 by additionally placing one insulating layer under the extending source electrode 30.

In the microstripline 40C, which connects the two intrinsic device sections 22a and 22b, the line width and the line length (= $\lambda/4$) thereof are selected such that the conditions for a λ/A transformer which achieves impedance matching with both intrinsic device sections 22a and 22b are satisfied.

According to the semiconductor device 71 having such a structure, a large power gain is obtained and the operating frequency can be increased. Fig. 11 is a chart showing the gain-frequency characteristics (indicated by a solid line) of a semiconductor device having a single-stage intrinsic device section 22 and the gain-frequency characteristics (indicated by a dotted line) of a semiconductor device having two-stage intrinsic device sections 22a and 22b. As shown in Fig. 11, whereas a usual millimeter-wave device has a power gain of about 6 dB at the 60 GHz band, a two-stage device has a power gain of about 12 dB at the 60 GHz and obtains a power gain of 6 dB at even near 90 GHz.

In the above embodiments, microstriplines, striplines, and coplanar lines are used as the micro-wave transmission lines at the input and output sections. Other lines may be used if they form a waveguide, such as an H line in which dielectric film is placed between the gate and source electrodes and between the drain and source electrodes.

Claims

1. A high-frequency semiconductor device (21; 51; 61; 71), wherein an intrinsic device section (22) is partially formed on a semiconductor substrate (21);

   a source electrode (29) and a drain electrode (31) are disposed in said intrinsic device section (22) with a gate electrode (36) placed therebetween;
   a micro-wave transmission line (40A) is formed between said gate electrode (36) or an electrode section (35) electrically connected to said gate electrode (36) and said source electrode (29) or an electrode section (30) electrically connected to said source electrode (29); and
   a micro-wave transmission line (40B) is formed between said drain electrode (31) or an electrode section (39) electrically connected to said drain electrode (31) and said source electrode (29) or an electrode section (30) electrically connected to said source electrode (29).

2. A high-frequency semiconductor device (21; 51; 61; 71), wherein an intrinsic device section (22) is partially formed on a semiconductor substrate (21);

   a source electrode (29) and a drain electrode (31) are disposed in said intrinsic device section (22) with a gate electrode (36) placed therebetween;
   said source electrode (29) or an electrode sec-

tion (30) electrically connected to said source electrode (29) covers most of said semiconductor substrate (21);

a micro-wave transmission line (40A) is formed by oppositely disposing said gate electrode (36) or an electrode section (35) electrically connected to said gate electrode (36) through a dielectric layer (34) above said source electrode (29) or an electrode section (30) electrically connected to said source electrode (29); and

a micro-wave transmission line (40A) is formed by oppositely disposing said drain electrode (31) or an electrode section (39) electrically connected to said drain electrode (31) through a dielectric layer (34) above said source electrode (29) or an electrode section (30) electrically connected to said source electrode (29).

3. A high-frequency semiconductor device (61; 71) according to one of Claims 1 and 2, wherein a plurality of said intrinsic device sections (22; 22a; 22b) are disposed on said semiconductor substrate (21) and said plurality of said intrinsic device sections are connected by micro-wave transmission lines (40A; 40B; 40C).

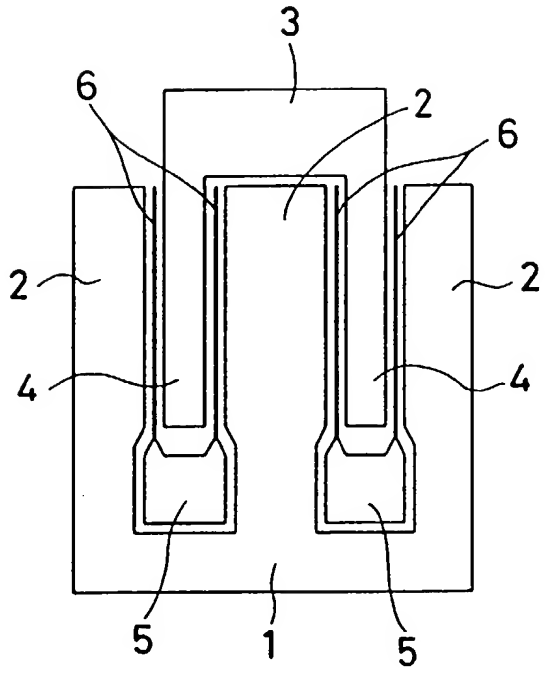

FIG. 1

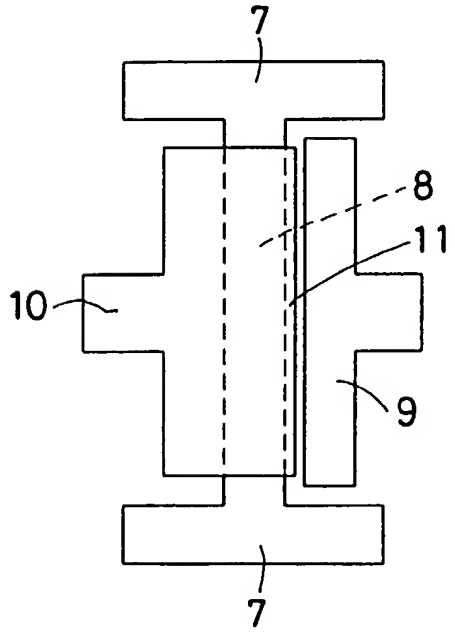

FIG. 2

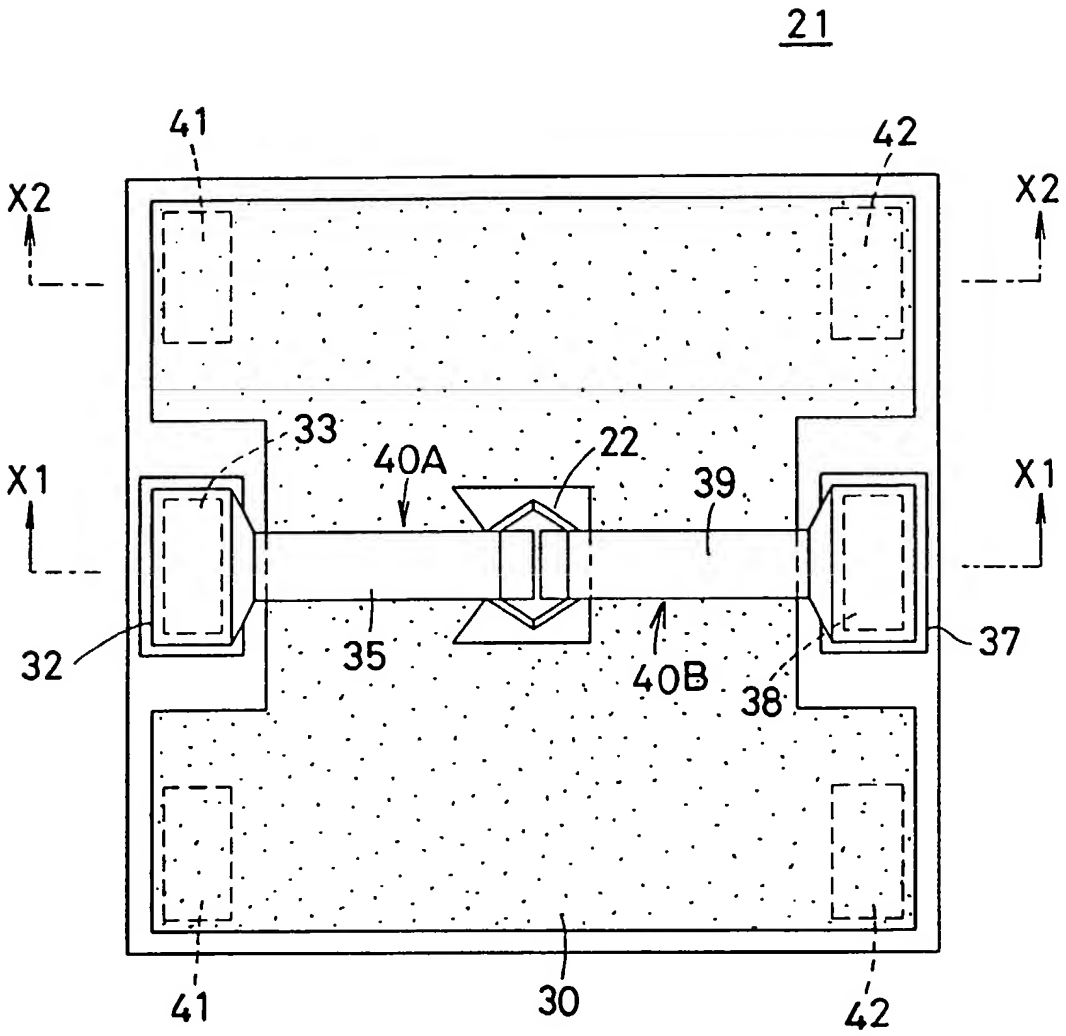

FIG. 3

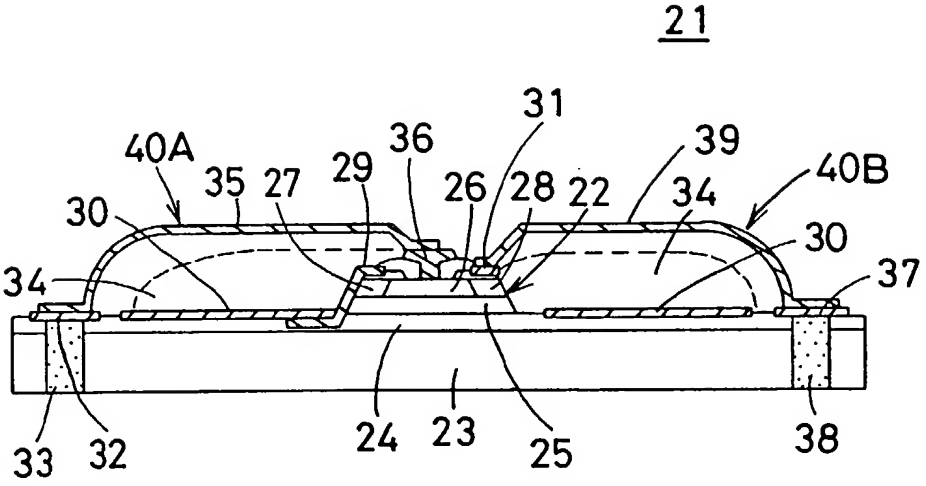
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FIG. 4

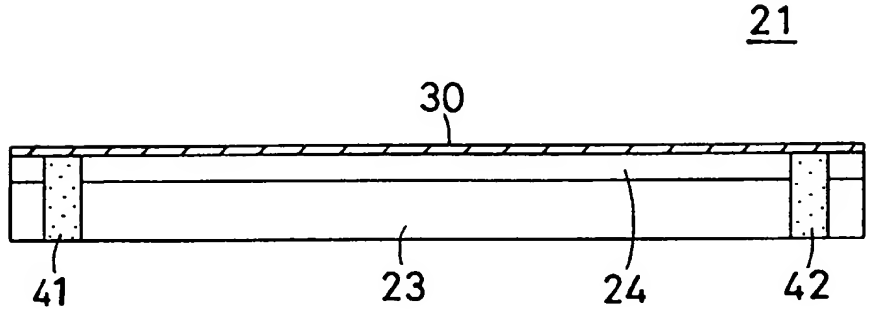
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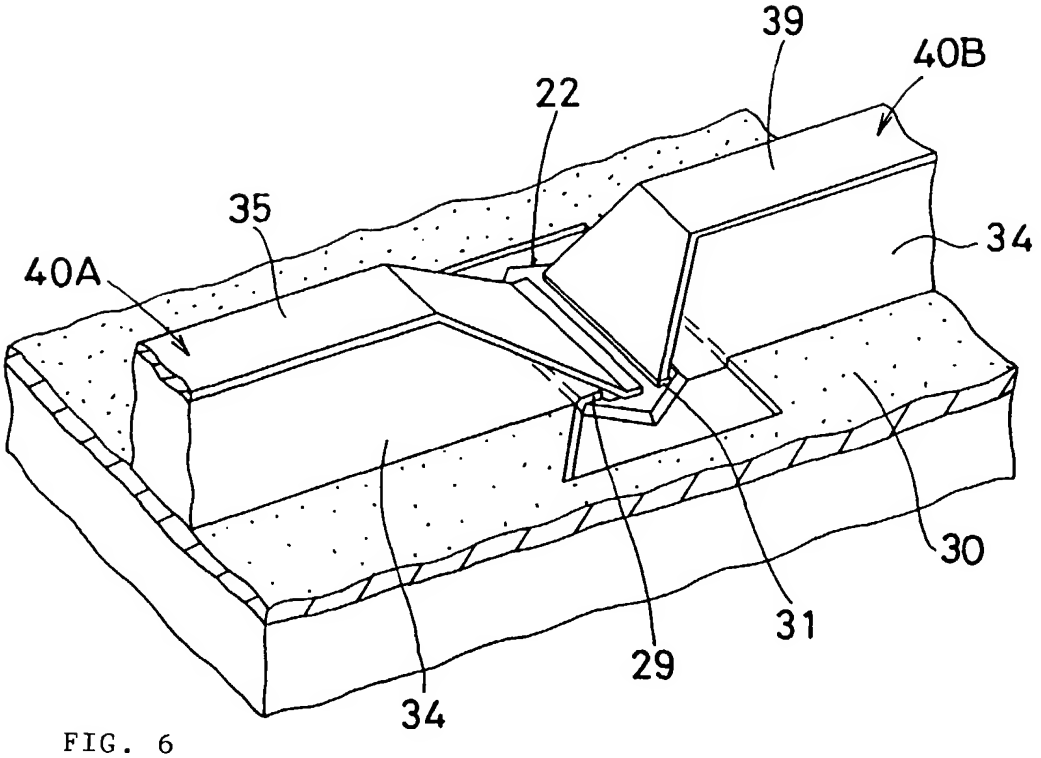
FIG. 5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40B
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40A
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FIG. 6

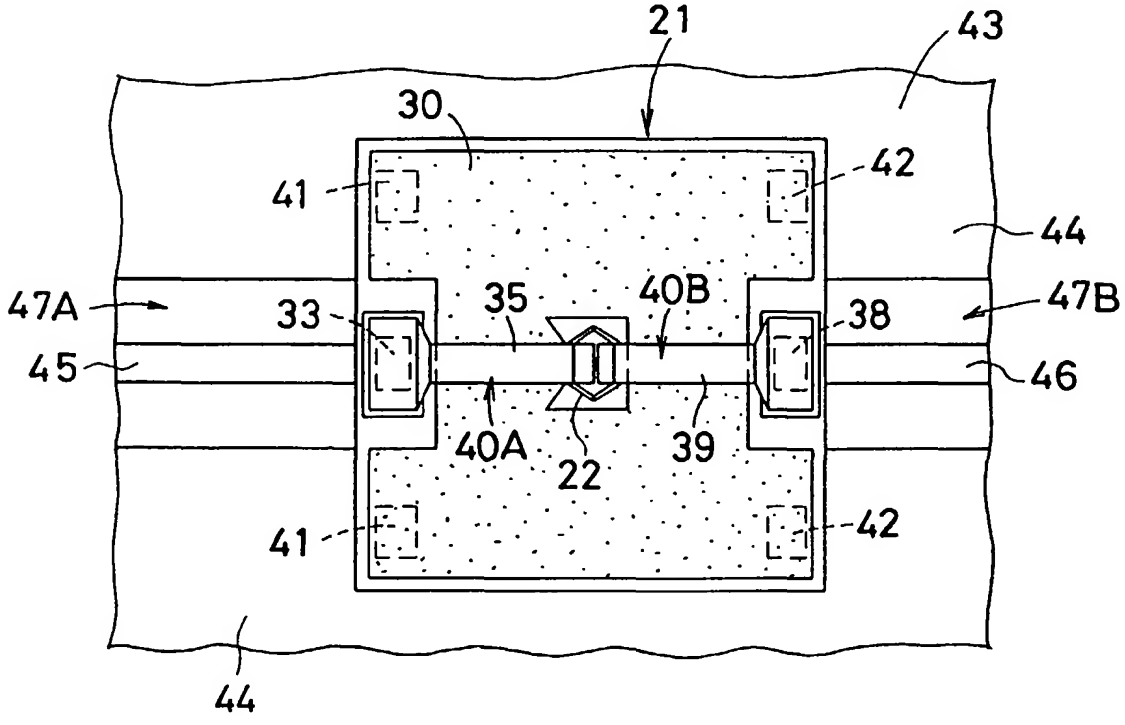
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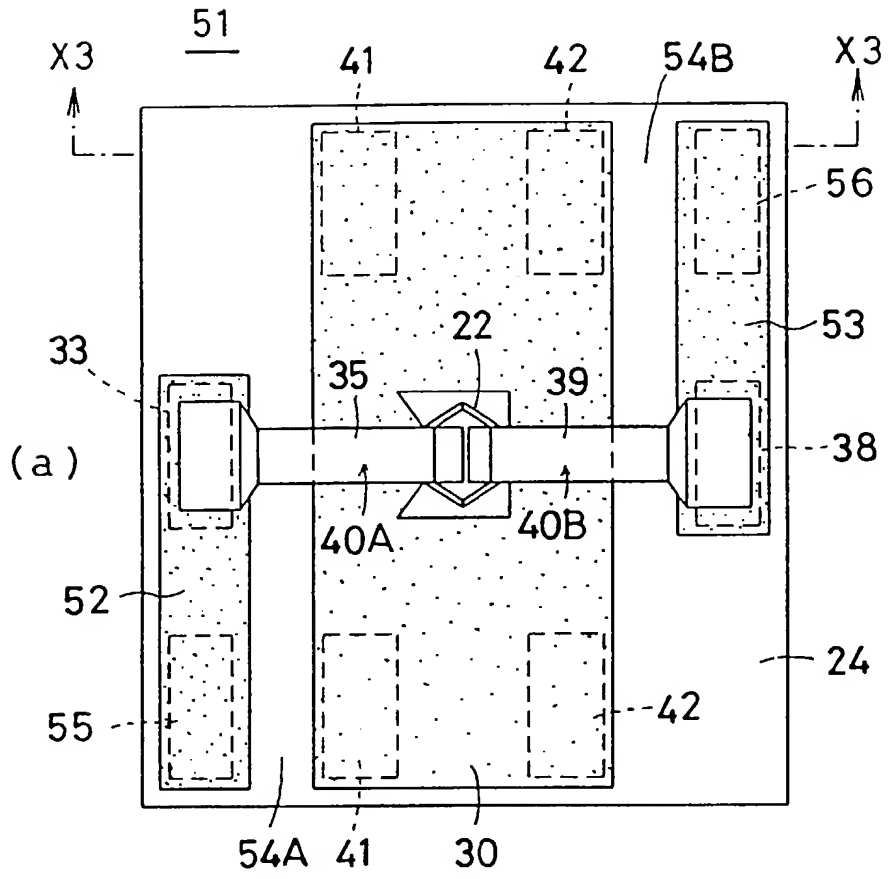
FIG. 7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41
30

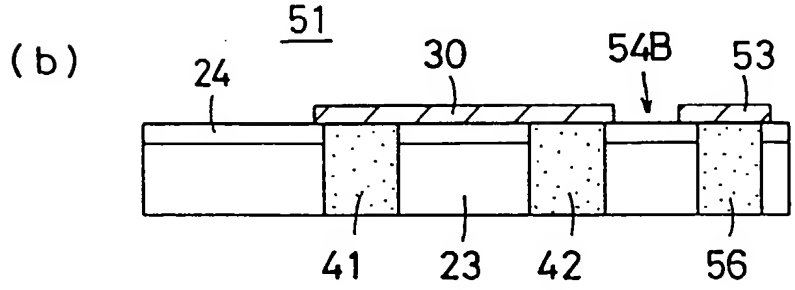
(b)
51
24
30
54B
53
41
23
42
56

FIG. 8

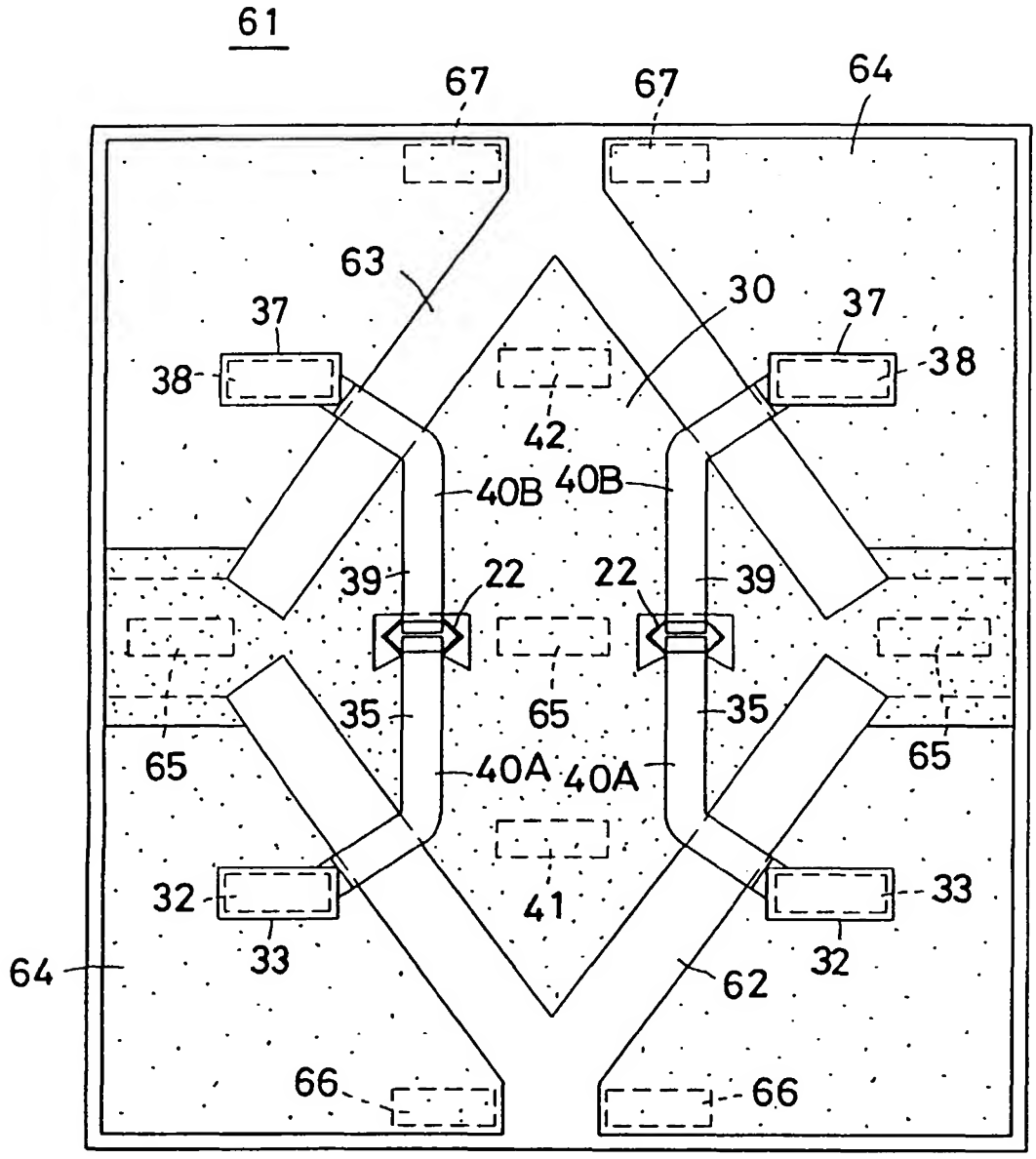
61
67
67
64
63
30
37
37
38
38
42
40B
40B
39
22
22
39
35
65
35
65
65
40A
40A
32
33
41
33
32
64
62
66
66

FIG. 9

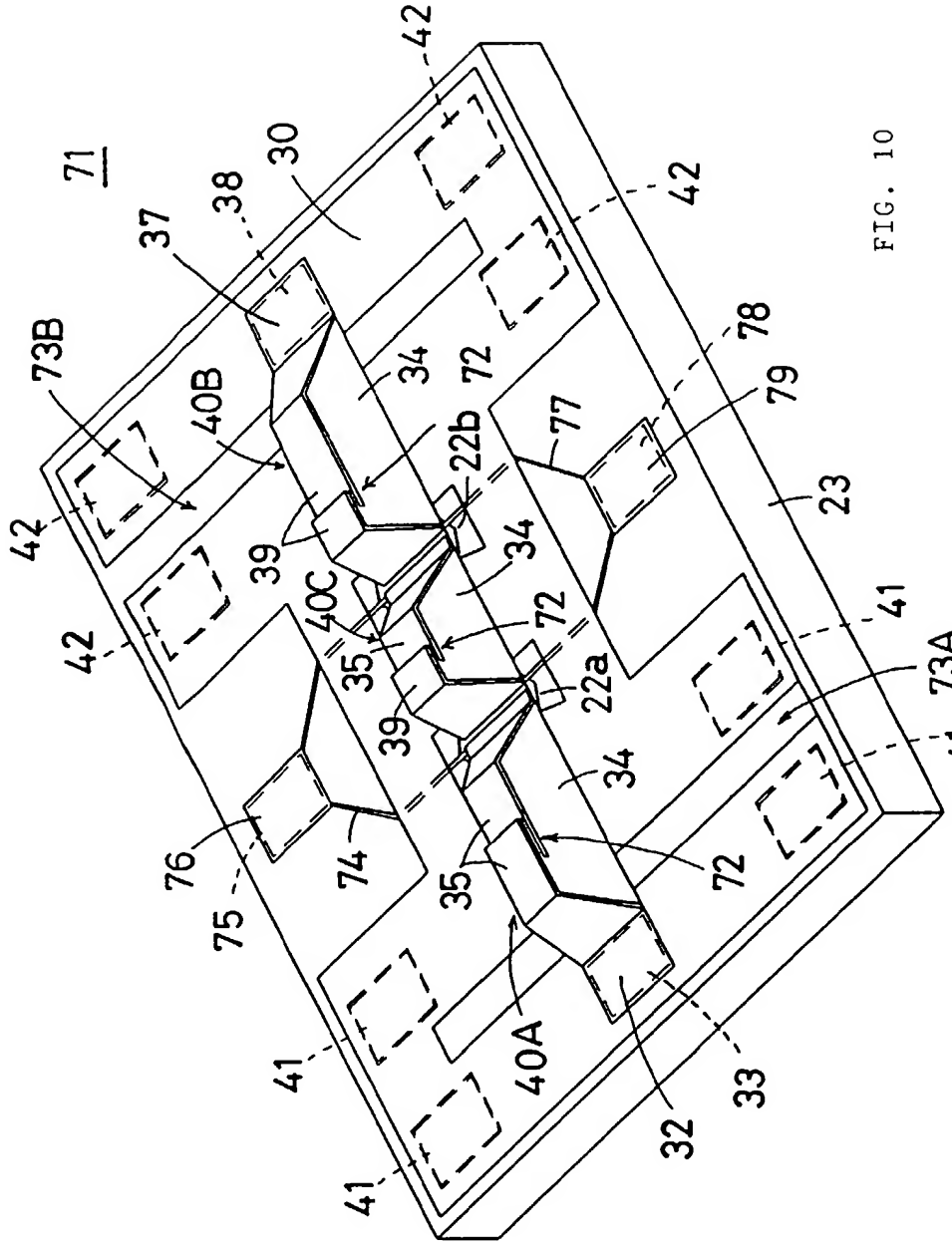
71
30
37
38
42
73B
40B
22b
77
78
79
23
39
40C
35
72
34
22a
73A
41
74
76
75
40A
32
33

FIG. 10

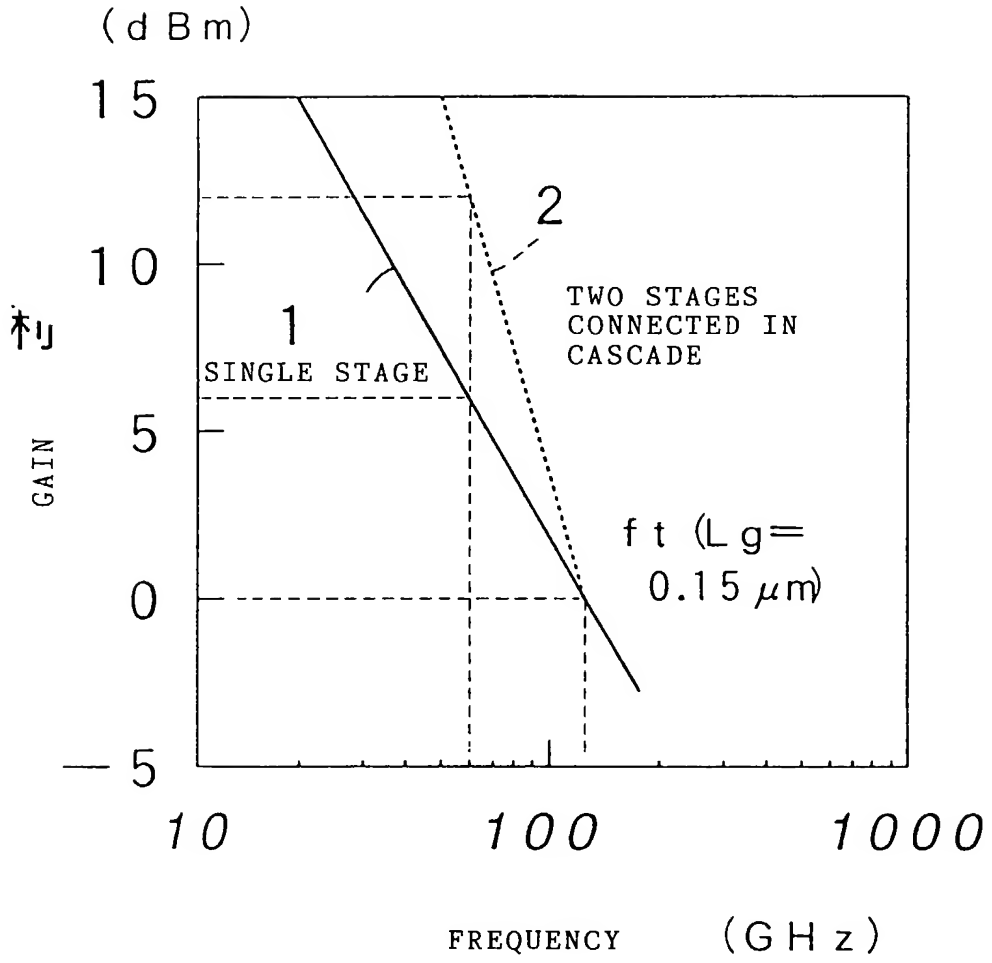
(dBm)
15
10
5
0
— 5
GAIN
利
1
SINGLE STAGE
2
TWO STAGES
CONNECTED IN
CASCADE
ft (Lg=
0.15 μm)
10
100
1000
FREQUENCY (GHz)

FIG. 11